Claims

[c1] 1. A method of fabricating a high performance copper (Cu) laminate inductor comprising:
forming a last metal Cu level of the Cu laminate inductor at the last metal level, which is defined as the last metal level beneath a bond pad level;
forming and superposing a bar via of the Cu laminate inductor over the last metal Cu level of the Cu laminate inductor;
forming and superposing a last metal + 1 Cu level of the Cu laminate inductor at the last metal + 1 level over the bar via and last metal Cu level, to form the Cu laminate inductor.

[c2] The method of claim 1, further comprising forming a passivating layer over the last metal + 1 Cu level of the Cu laminate inductor.

[c3] The method of claim 2, further comprising forming a passivating layer of CoWP over the last metal + 1 Cu level of the Cu laminate inductor.

[c4] The method of claim 1, for forming a Cu inductor having an aluminum bond pad, further comprising the steps of:

a. forming last metal layer damascene Cu interconnects in a dielectric;
b. depositing one or more layers of passivation material over the last metal layer damascene Cu interconnects;
c. patterning terminal vias in the one or more layers of passivation material;
d. depositing metal for bond pads and a barrier layer, patterning the metal for bond pads and barrier layer, and depositing a Cu seed layer;
e. depositing and patterning a resist for Cu inductors, and depositing Cu to selectively form Cu in inductor regions;
f. stripping the resist, etching the Cu seed layer, and selectively depositing a passivating layer on Cu inductors.

[c5] The method of claim 4, further including:
g. after step f, coating the structure of step f with polyimide, and forming openings to bond pads.
h. depositing barrier layer metallurgy, and forming solder balls.

[c6] The method of claim 1, for forming a Cu inductor having a Cu bond pad, further comprising the steps of:
a. forming last metal layer damascene Cu interconnects in a dielectric;
b. depositing one or more layers of passivation material over the last metal layer damascene Cu interconnects;

c. patterning terminal vias in the one or more layers of passivation material;
d. depositing a barrier layer and Cu seed layer;
e. depositing and patterning a resist for Cu inductors, and depositing Cu to selectively form Cu in inductor regions;
f. stripping the resist, etching the Cu seed layer, and selectively depositing a passivating layer on Cu inductors and terminals.

[c7] The method of claim 6, further including:
g. after step f, coating the structure of step f with polyimide, and forming openings to bond pads.
h. depositing barrier layer metallurgy, and forming solder balls.

[c8] 8. The method of claim 1, for forming a Cu inductor having a raised Cu bond pad, further comprising the steps of:
a. forming last metal layer damascene Cu interconnects in a dielectric;
b. depositing one or more layers of passivation material over the last metal layer damascene Cu interconnects;
c. patterning terminal vias in the one or more layers of passivation material;
d. depositing a barrier layer and Cu seed layer;
e. depositing and patterning a resist for Cu inductors,

terminals and interconnect wiring, and depositing Cu to selectively form Cu in unmasked regions;
f. stripping the resist, etching the Cu seed layer, and selectively depositing a passivating layer on Cu inductors, terminals and interconnect wiring.

[c9] The method of claim 8, further including:
g. after step f, coating the structure of step f with polyimide, and forming openings to bond pads.
h. depositing barrier layer metallurgy, and forming solder balls.

[c10] The method of claim 1, further including depositing a Cu seed layer before depositing and patterning resist, followed by selective deposition of Cu, comprising:
a. after a terminal via etch, depositing a barrier layer, and depositing the Cu seed layer;
b. depositing and patterning resist for inductors, terminals and interconnects, and depositing Cu by electroplating to selectively form Cu in inductor, terminal and interconnect regions;
c. stripping the resist and etching the Cu seed layer and the barrier layer.

[c11] The method of claim 1, further including depositing a Cu seed layer after depositing and patterning resist, followed by blanket deposition of Cu and chemical me-

chanical polishing, comprising:

a. after a terminal via etch, depositing a barrier layer;

b. depositing and patterning resist for inductors, terminals and interconnects, and depositing Cu seed layer;

c. depositing Cu;

d. removing excess Cu;

e. stripping the resist and etching the barrier layer.

[c12] The method of claim 1, further including depositing a barrier layer and Cu seed layer after depositing and patterning resist, followed by blanket deposition of a barrier layer and Cu and chemical mechanical polishing, comprising:

a. after a terminal via etch;

b. depositing and patterning resist for inductors, terminals and interconnects, depositing a barrier adhesion layer, and depositing Cu seed layer;

c. depositing Cu;

d. removing excess Cu, removing the barrier adhesion layer;

e. stripping the resist and etching the barrier layer.

[c13] The method of claim 1, further including selectively depositing a passivating metal.

[c14] The method of claim 1, further including selectively depositing a passivating dielectric.

[c15] The method of claim 1, further including selectively depositing a passivating metal and a passivating dielectric.

[c16] The method of claim 1, further including selectively depositing a passivating metal or a passivating dielectric, etching back to form spacers, deposit dielectric layer.

[c17] The method of claim 1, further including selectively depositing a passivating metal or a passivating dielectric, etching back to form spacers, deposit selective metal on Cu.

[c18] The method of claim 1, further including selectively depositing a passivating metal or a passivating dielectric, deposit selective metal on Cu, etching back to form spacers, deposit dielectric layer.